

### Product Overview

NSI1312 is a cost-effective isolated amplifier with output separated from input based on the NOVOSENSE capacitive isolation technology Adaptive OOK®. The device has a linear differential input signal range of  $\pm 1.2V$  ( $\pm 1.5V$  full-scale). The high input impedance of NSI1312 makes it highly suitable for connection to high-voltage resistive dividers or other voltage signal sources with high output resistance.

The device has a fixed gain of 1 and provides differential analog output version (NSI1312D) and single-ended analog output version (NSI1312S) option.

The low offset and gain drift ensure the accuracy over the entire temperature range. The high common-mode transient immunity ensures that the device is able to provide accurate and reliable measurements even in the presence of high-power switching such as in motor control applications.

The fail-safe function (missing VDD1 detection) simplifies system-level design and diagnostics.

### Key Features

- Up to 5000V<sub>RMS</sub> Insulation Voltage
- $\pm 1.2V$  Linear Input Voltage Range
- Fixed Gain : 1
- Excellent DC Performance:
  - Offset Error:  $\pm 2.5mV$  (Max)
  - Offset Drift:  $\pm 20\mu V/^\circ C$  (Max)
  - Gain Error:  $\pm 0.3\%$  (Max)
  - Gain Error Drift:  $\pm 40ppm/^\circ C$  (Max)
  - Nonlinearity:  $\pm 0.05\%$  (Max)
  - Nonlinearity Drift:  $\pm 1ppm/^\circ C$  (Typ)
- SNR: 78dB (Typ)
- High CMTI: 150kV/ $\mu s$  (Typ)
- System-Level Diagnostic Features:
  - VDD1 monitoring
- Operation Temperature:  $-40^\circ C \sim 125^\circ C$

- RoHS-Compliant Packages:
  - SOW8 wide body (SOP8 300mil)
  - SOP8 narrow body (SOP8 150mil)

### Safety Regulatory Approvals

- UL recognition:
  - SOW8: 5000V<sub>rms</sub> for 1 minute per UL1577
  - SOP8: 3000V<sub>rms</sub> for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

### Applications

- AC motor controls
- Power and solar inverters
- Uninterruptible Power Suppliers
- Automotive onboard chargers

### Device Information

Part Number	Package	Body Size
NSI1312x-DSWVR	SOW8(300mil)	5.85mm × 7.50mm
NSI1312x-DSPR	SOP8(150mil)	4.90mm × 3.90mm

### Functional Block Diagrams

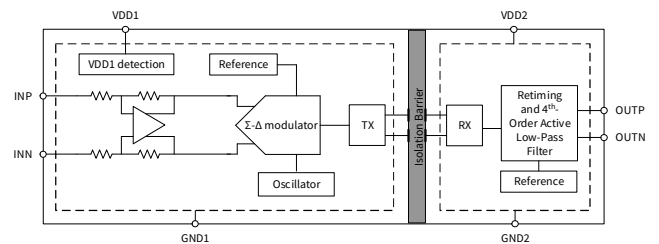


Figure 1. NSI1312D Block Diagram

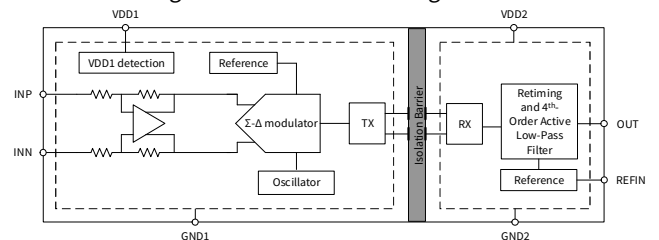


Figure 2. NSI1312S Block Diagram

**INDEX**

**1. PIN CONFIGURATION AND FUNCTIONS..... 3**

**2. ABSOLUTE MAXIMUM RATINGS ..... 5**

**3. ESD RATINGS ..... 5**

**4. RECOMMENDED OPERATING CONDITIONS ..... 5**

**5. THERMAL INFORMATION..... 5**

**6. SPECIFICATIONS..... 6**

**6.1. ELECTRICAL CHARACTERISTICS..... 6**

**6.2. POWER RATING CHARACTERISTICS ..... 7**

**6.3. TYPICAL PERFORMANCE CHARACTERISTICS ..... 8**

**6.4. PARAMETER MEASUREMENT INFORMATION ..... 11**

**7. HIGH VOLTAGE FEATURE DESCRIPTION..... 11**

**7.1. INSULATION AND SAFETY RELATED SPECIFICATIONS ..... 11**

**7.2. INSULATION CHARACTERISTICS..... 12**

**7.3. REGULATORY INFORMATION ..... 13**

**8. FUNCTION DESCRIPTION ..... 14**

**8.1. OVERVIEW ..... 14**

**8.2. ANALOG INPUT ..... 15**

**8.3. ANALOG OUTPUT..... 15**

**9. APPLICATION NOTE ..... 17**

**9.1. TYPICAL APPLICATION CIRCUIT ..... 17**

**9.2. SENSE RESISTOR SELECTION ..... 17**

**9.3. PCB LAYOUT ..... 18**

**10. PACKAGE INFORMATION ..... 18**

**11. ORDERING INFORMATION ..... 21**

**12. DOCUMENTATION SUPPORT ..... 21**

**13. TAPE AND REEL INFORMATION ..... 22**

**14. REVISION HISTORY..... 24**

## 1. Pin Configuration and Functions

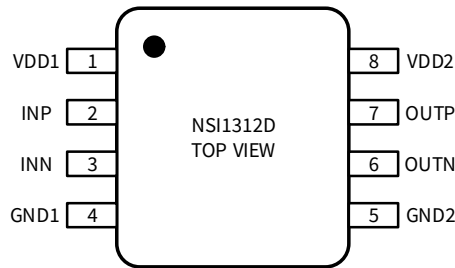


Figure 1.1 NSI1312D Package (SOW8 and SOP8)

Table 1.1 NSI1312D Pin Configuration and Description

<b>NSI1312D PIN NO.</b>	<b>SYMBOL</b>	<b>FUNCTION</b>
1	VDD1	Power supply for isolator input side (3.0V to 5.5V)
2	INP	Positive analog input
3	INN	Negative analog input
4	GND1	Ground 1, the ground reference for input side
5	GND2	Ground 2, the ground reference for output side
6	OUTN	Negative output
7	OUTP	Positive output
8	VDD2	Power supply for isolator output side (3.0V to 5.5V)

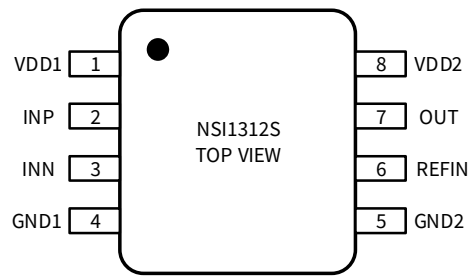


Figure 1.2 NSI1312S Package (SOW8 and SOP8)

Table 1.2 NSI1312S Pin Configuration and Description

<b>NSI1312S PIN NO.</b>	<b>SYMBOL</b>	<b>FUNCTION</b>
1	VDD1	Power supply for input side (3.0V to 5.5V)
2	INP	Positive analog input
3	INN	Negative analog input
4	GND1	Ground 1, the ground reference for input side
5	GND2	Ground 2, the ground reference for output side
6	REFIN	External Reference Input
7	OUT	Output
8	VDD2	Power supply for output side (3.0V to 5.5V)

## 2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VDD1, VDD2	-0.3		6.5	V
Input Voltage	INP, INN	GND1-6		VDD1+0.5	V
	REFIN	GND2-0.5		VDD2+0.5	V
Output Voltage	OUTP, OUTN, OUT	GND2-0.5		VDD2+0.5	V
Output current per Output Pin	I <sub>o</sub>	-10		10	mA
Junction Temperature	T <sub>J</sub>	-40		150	°C
Storage Temperature	T <sub>STG</sub>	-55		150	°C

## 3. ESD Ratings

Parameters	Test Condition	Value	Unit
Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4.0	kV
	Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1.0	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Input side Power Supply	VDD1	3.0	5.0	5.5	V
Output side Power Supply	VDD2	3.0	3.3	5.5	V
Differential input voltage before clipping output	V <sub>Clipping</sub>		±1.5		V
Linear differential input full scale voltage	V <sub>FSR</sub>	-1.2		1.2	V
Operating common-mode input voltage	V <sub>CM</sub>	-0.8		0.8	V
Operating Ambient Temperature	T <sub>A</sub>	-40		125	°C

## 5. Thermal Information

Parameters	Symbol	SOW8	SOP8	Unit
Junction-to-ambient thermal resistance	R <sub>θJA</sub>	86	137.7	°C/W
Junction-to-case (top) thermal resistance	R <sub>θJC(top)</sub>	28	54.9	°C/W
Junction-to-board thermal resistance	R <sub>θJB</sub>	42	71.7	°C/W
Junction-to-top characterization parameter	Ψ <sub>JT</sub>	4	12	°C/W
Junction-to-board characterization parameter	Ψ <sub>JB</sub>	42	46	°C/W

## 6. Specifications

### 6.1. Electrical Characteristics

(AVDD = 3.0V ~ 5.5V, DVDD = 3.0V ~ 5.5V, INP = -1.2V to +1.2V, and INN = AGND = 0V, T<sub>A</sub> = -40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 3.3V, T<sub>A</sub> = 25°C. Output characteristics is based on OUTP-OUTN for NSI1312D, is based on OUT-REFIN for NSI1312S.)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
<b>Power Supply</b>						
Input side supply voltage	VDD1	3.0	5.0	5.5	V	
Output side supply voltage	VDD2	3.0	3.3	5.5	V	
Input side supply current	IDD1		7.2	9	mA	
Output side supply current	IDD2		4.7	6.2	mA	
VDD1 undervoltage detection threshold voltage	VDD1 <sub>UV</sub>	1.8	2.3	2.7	V	VDD1 falling
<b>Analog Input</b>						
Input offset voltage	V <sub>OS</sub>	-2.5	±1	2.5	mV	INP = INN = GND1, at T <sub>A</sub> = 25°C
Input offset drift	TCV <sub>OS</sub>	-20	0.5	20	μV/°C	
Common-mode rejection ratio	CMRR <sub>dc</sub>		-80		dB	INP = INN, f <sub>IN</sub> = 0 Hz, V <sub>CM min</sub> ≤ VIN ≤ V <sub>CM max</sub>
	CMRR <sub>ac</sub>		-82		dB	INP = INN, f <sub>IN</sub> = 10 kHz, V <sub>CM min</sub> ≤ VIN ≤ V <sub>CM max</sub>
Single-ended input resistance	R <sub>IN</sub>		1		MΩ	INN = GND1
Differential input resistance	R <sub>IND</sub>		1.6		MΩ	
Input capacitance	C <sub>i</sub>		2		pF	
Input bias current	I <sub>IB</sub>	-0.7	-0.6	-0.5	μA	INP = INN = GND1, at T <sub>A</sub> = 25°C, I <sub>IB</sub> = (I <sub>IBP</sub> + I <sub>IBN</sub> ) / 2
Input bias current drift	TCI <sub>IB</sub>		-1		nA/°C	
<b>Analog Output</b>						
Nominal Gain			1		V/V	
Gain error	E <sub>G</sub>	-0.3%	±0.1%	0.3%		at T <sub>A</sub> = 25°C
Gain error thermal drift	TCE <sub>G</sub>	-40	-10	40	ppm/°C	
Nonlinearity		-0.05%	±0.01%	0.05%		at T <sub>A</sub> = 25°C
Nonlinearity drift			±1		ppm/°C	
Total harmonic distortion	THD		-75		dB	V <sub>IN</sub> = ±1.2V, f <sub>IN</sub> = 10kHz, BW = 50kHz
Output noise			100		μV <sub>RMS</sub>	INP = INN = GND1, BW = 50kHz
Signal to noise ratio	SNR		78		dB	V <sub>IN</sub> = ±1.2V, f <sub>IN</sub> = 10kHz, BW = 50kHz

Common-mode output voltage	$V_{CMout}$	1.39	1.44	1.49	V	Only for NSI1312D
Differential fail-safe output voltage	$V_{FAILSAFE}$		-1.8	-1.7	V	NSI1312D VDD1 missing
Single-ended fail-safe output voltage	$V_{FAILSAFE}$		0		V	NSI1312S VDD1 missing, REFIN<1.8V
			REFIN-1.8		V	NSI1312S VDD1 missing, REFIN>1.8V
Single-ended reference input	REFIN	0.5	VDD2/2	VDD2-1.5	V	Only for NSI1312S. See application description for more details.
Single-ended reference input impedance	REFIN <sub>IN</sub>		1		GΩ	Only for NSI1312S
Output bandwidth	BW	50	100		kHz	
Power supply rejection ratio	PSRR <sub>dc</sub>		-95		dB	PSRR vs VDD1, at DC
	PSRR <sub>ac</sub>		-95		dB	PSRR vs VDD1, 100mV and 10kHz ripple
	PSRR <sub>dc</sub>		-90		dB	PSRR vs VDD2, at DC
	PSRR <sub>ac</sub>		-80		dB	PSRR vs VDD2 for NSI1312D, 100mV and 10kHz ripple
	PSRR <sub>ac</sub>		-72		dB	PSRR vs VDD2 for NSI1312S, 100mV and 1kHz ripple
Output resistance	R <sub>OUT</sub>		< 0.2		Ω	
Output limit current	I <sub>LIM</sub>		±13		mA	
Common-mode transient immunity	CMTI	100	150		kV/μs	Common-mode transient immunity
<b>Timing</b>						
Rising time of OUTP, OUTN	t <sub>r</sub>		3.6		μs	
Falling time of OUTP, OUTN	t <sub>f</sub>		3.6		μs	
INP, INN to OUTP, OUTN signal delay (50% - 50%)	t <sub>PD</sub>		3.5	4	μs	
Analog settling time	t <sub>AS</sub>		0.5		ms	VDD1 step to 5.0 V with VDD2 ≥ 3.0 V, to OUTP, OUTN valid, 0.1% settling

**6.2. Power Rating Characteristics**

Parameters	Symbol	Max	Unit	Comments
Total Power dissipation	P <sub>D</sub>	83.6	mW	VDD1=VDD2=5.5V
Power dissipation of high side	P <sub>D1</sub>	49.5	mW	VDD1=5.5V
Power dissipation of low side	P <sub>D2</sub>	34.1	mW	VDD2=5.5V

### 6.3. Typical Performance Characteristics

Unless otherwise noted, test at NSI1312D VDD1 = 5V, VDD2 = 3.3V, INN=GND1=0V, INP = -1.2V to 1.2V,  $f_{in}$  = 1kHz, BW = 10kHz. Characteristics of NSI1312S may be related to REFIN accuracy.

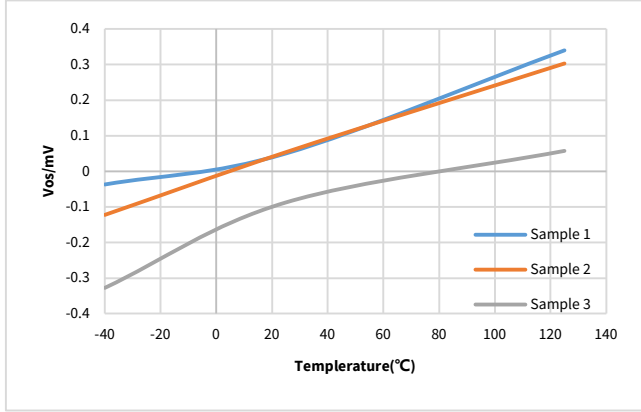


Figure 6.1 Input Offset Voltage vs Temperature

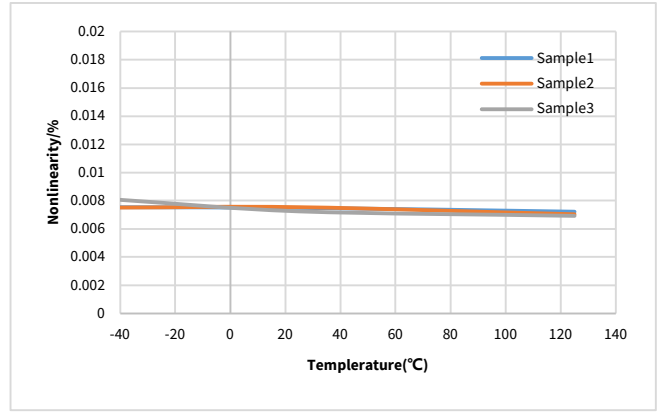


Figure 6.3 Nonlinearity vs Temperature

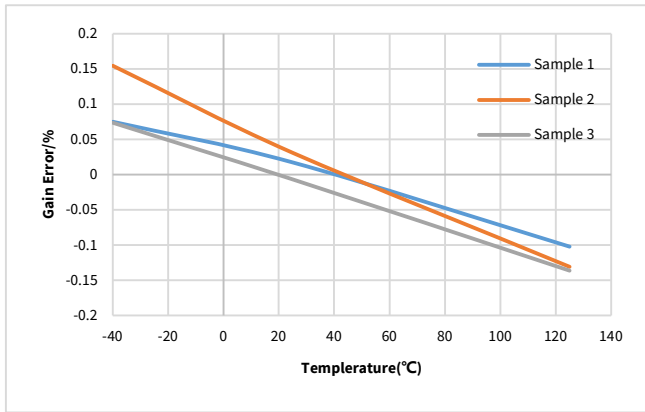


Figure 6.2 Gain Error vs Temperature

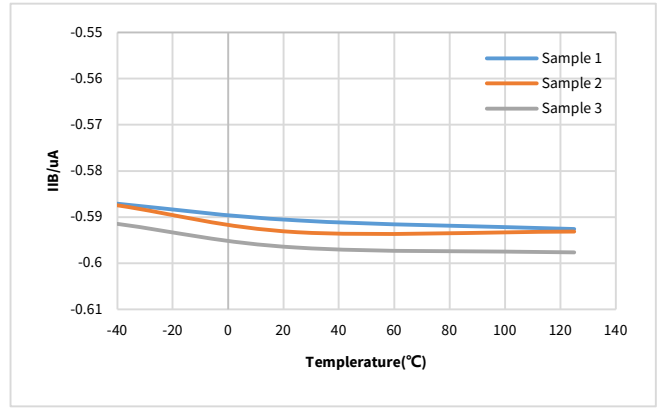


Figure 6.4 Input Bias Current vs Temperature

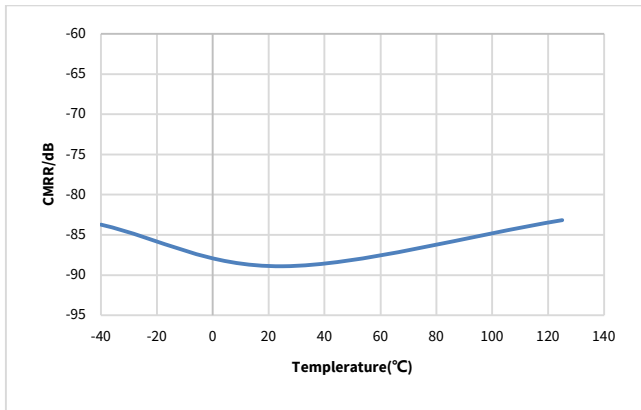


Figure 6.5 Common-Mode Rejection Ratio vs Temperature

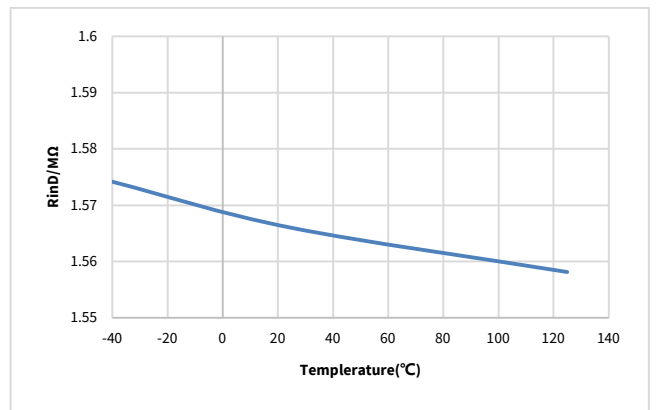


Figure 6.6 Differential Input Resistance vs Temperature



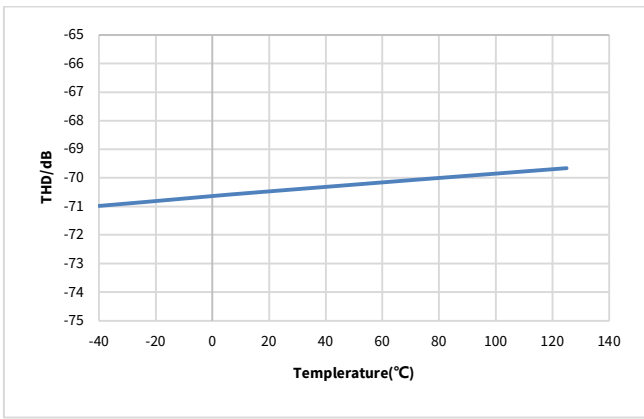


Figure 6.7 THD vs Temperature

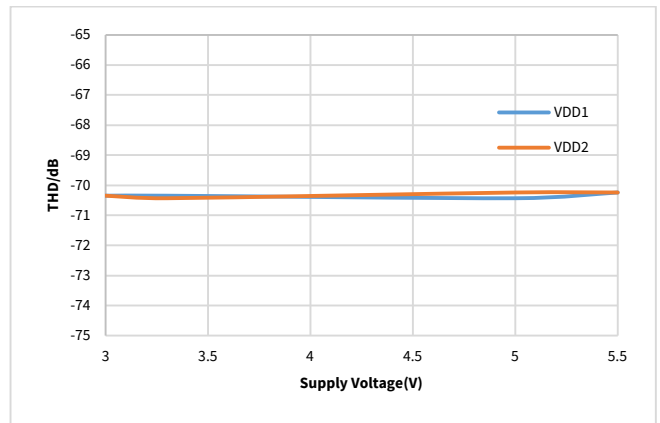


Figure 6.8 THD vs Supply Voltage

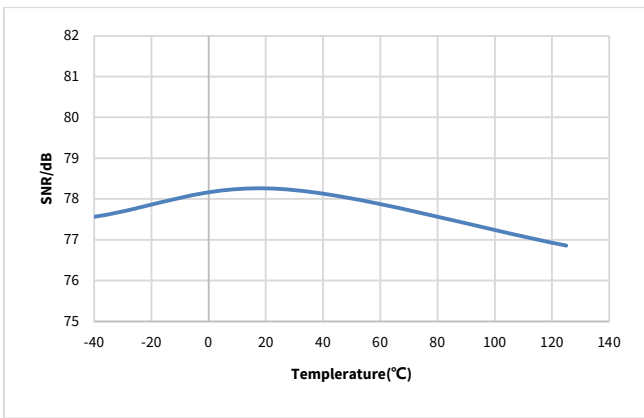


Figure 6.9 SNR vs Temperature

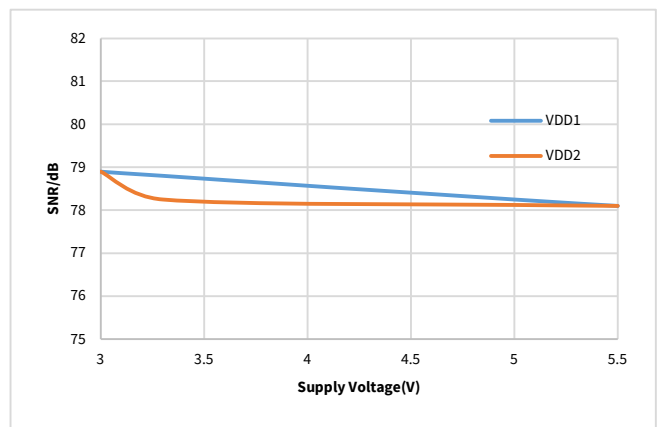


Figure 6.10 SNR vs Supply Voltage

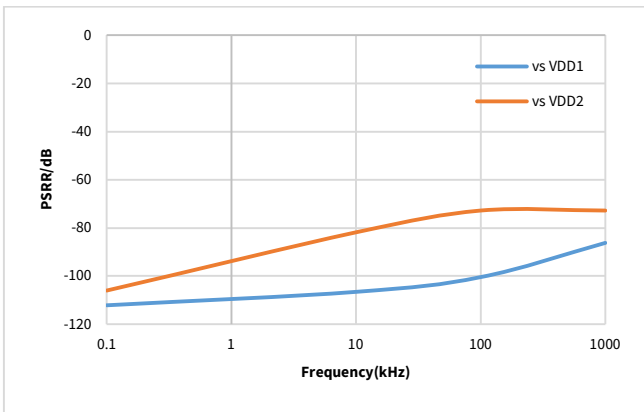


Figure 6.11 Power-Supply Rejection Ratio vs Ripple Frequency (NSI1312D)

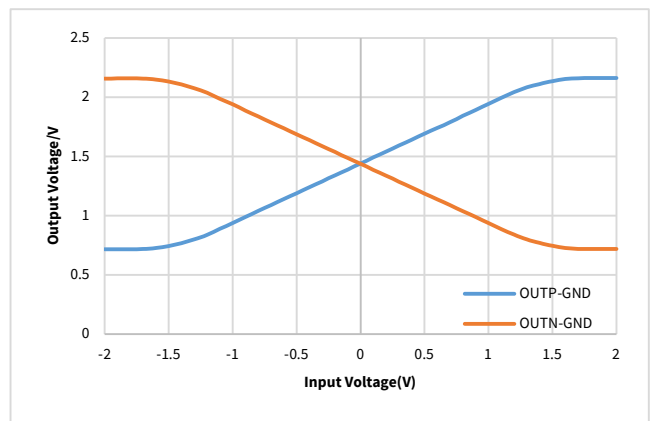


Figure 6.12 Output Voltage vs Input Voltage (NSI1312D)

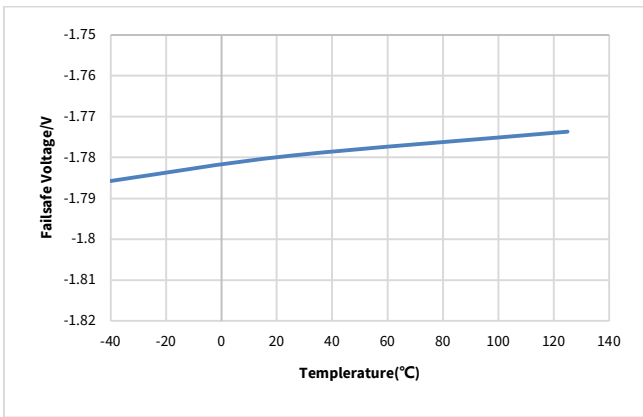


Figure 6.13 Fail-Safe Output Voltage vs Temperature (NSI1312D)

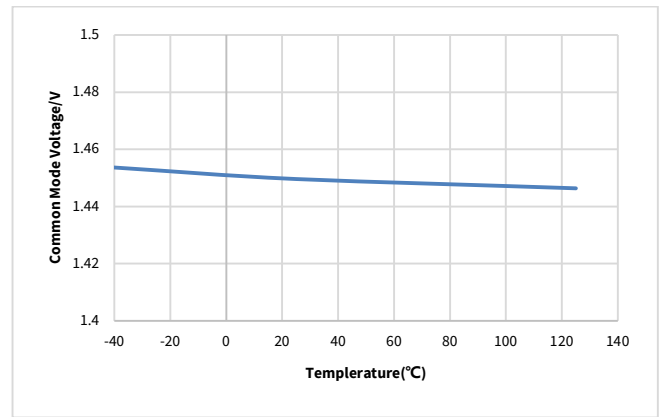


Figure 6.14 Output Common-Mode Voltage vs Temperature (NSI1312D)

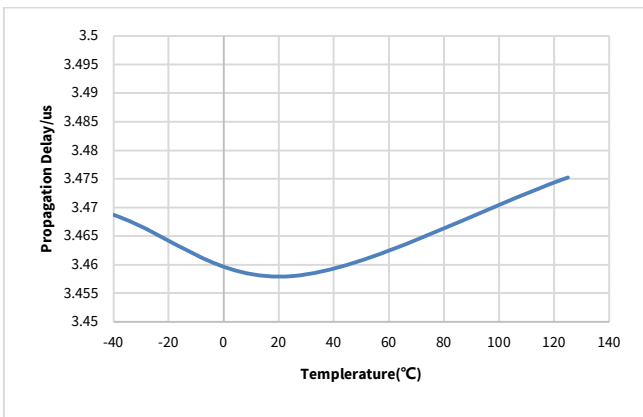


Figure 6.15 Vin to Vout Delay vs Temperature

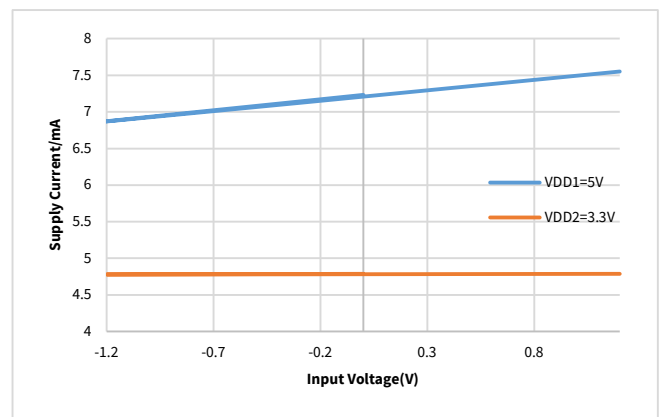


Figure 6.16 Supply Current vs Input Voltage

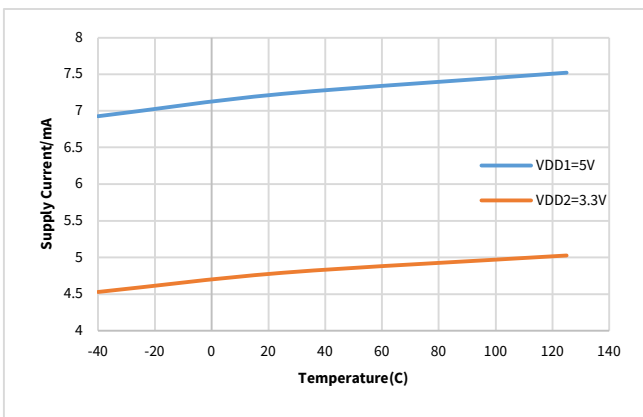


Figure 6.17 Supply Current vs Temperature

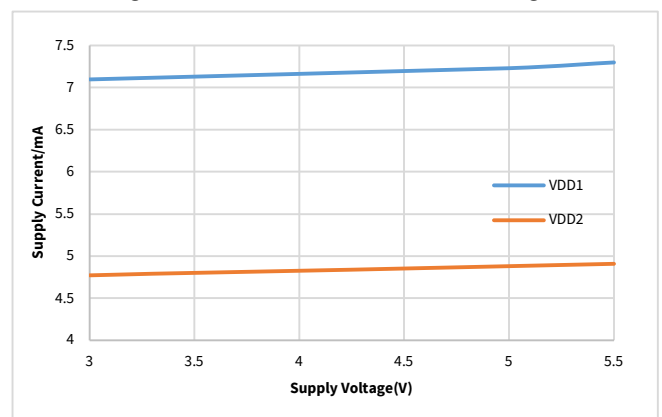


Figure 6.18 Supply Current vs Supply Voltage

6.4. Parameter Measurement Information

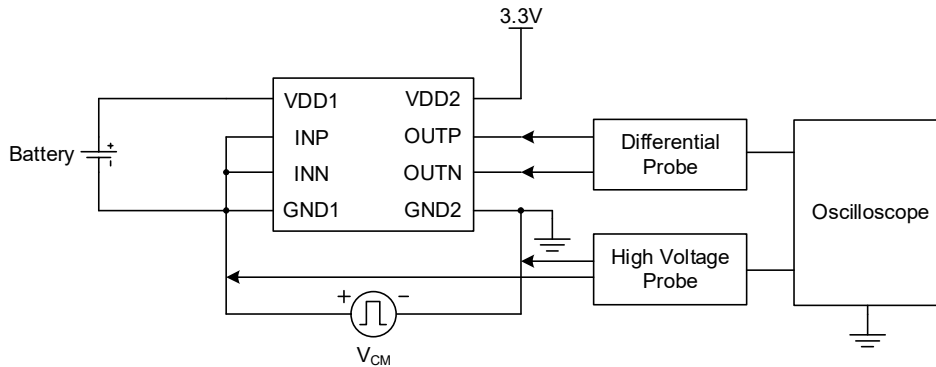


Figure 6.19 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value		Unit	Comments
		SOP8	SOW8		
Minimum External Clearance	CLR	4	8	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	4	8	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	28		µm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600		V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I			IEC 60664-1

Description	Test Condition	Value	
		SOP8	SOW8
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to IV	I to IV
	For Rated Mains Voltage ≤ 300Vrms	I to III	I to IV
	For Rated Mains Voltage ≤ 600Vrms	I to II	I to IV
	For Rated Mains Voltage ≤ 1000Vrms	I	I to III
Climatic Classification		40/125/21	
Pollution Degree per DIN VDE 0110		2	

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value		Unit
			SOP8	SOW8	
<b>DIN EN IEC 60747-17 (VDE 0884-17)</b>					
Maximum repetitive isolation voltage		$V_{IORM}$	990	2121	$V_{PEAK}$
Maximum working isolation voltage	AC Voltage	$V_{IOWM}$	700	1500	$V_{RMS}$
	DC Voltage		990	2121	$V_{DC}$
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}, t_{ini}=60\text{ s}, V_{pd(m)}=1.2*V_{IORM}, t_m=10\text{ s}.$	$q_{pd}$	/	<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}, t_{ini}=60\text{ s}, V_{pd(m)}=1.6*V_{IORM}, t_m=10\text{ s}$				pC
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}, t_{ini}=1\text{ s}$ $V_{pd(m)}=1.875*V_{IORM}, t_m=1\text{ s}$ (method b1) or $V_{pd(m)}=V_{ini}, t_m=t_{ini}$ (method b2)				pC
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}, t_{ini}=60\text{ s}, V_{pd(m)}=1.2*V_{IORM}, t_m=10\text{ s}.$	$q_{pd}$	<5	/	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}, t_{ini}=60\text{ s}, V_{pd(m)}=1.3*V_{IORM}, t_m=10\text{ s}$				pC
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}, t_{ini}=1\text{ s}$ $V_{pd(m)}=1.5*V_{IORM}, t_m=1\text{ s}$ (method b1) or $V_{pd(m)}=V_{ini}, t_m=t_{ini}$ (method b2)				pC
Maximum transient isolation voltage	$t = 60\text{ sec}$	$V_{IOTM}$	4242	8000	$V_{PEAK}$
Maximum impulse voltage	Tested in air, 1.2/50-us waveform per IEC62368-1	$V_{IMP}$	3000	6250	$V_{PEAK}$
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	$V_{IOSM}$	6000	10000	$V_{PEAK}$
Isolation resistance	$V_{IO} = 500\text{ V}, T_{amb} = 25^\circ\text{ C}$	$R_{IO}$	$>10^{12}$	$>10^{12}$	$\Omega$
	$V_{IO} = 500\text{ V}, 100^\circ\text{ C} \leq T_{amb} \leq 125^\circ\text{ C}$	$R_{IO}$	$>10^{11}$	$>10^{11}$	$\Omega$
	$V_{IO} = 500\text{ V}, T_{amb} = T_s$	$R_{IO}$	$>10^9$	$>10^9$	$\Omega$
Isolation capacitance	$f = 1\text{ MHz}$	$C_{IO}$	0.8	0.8	pF
Safety total power dissipation	$V_I = 5.5\text{ V}, T_J = 150^\circ\text{ C}, T_A = 25^\circ\text{ C}$	$P_s$	907	1453	mW

Description	Test Condition	Symbol	Value		Unit
			SOP8	SOW8	
Safety input, output, or supply current	$\theta_{JA} = 137.7^{\circ}\text{C/W}$ for SOP8, $V_I = 5.5\text{V}$ , $T_J = 150^{\circ}\text{C}$ , $T_A = 25^{\circ}\text{C}$	Is	165	/	mA
	$\theta_{JA} = 86^{\circ}\text{C/W}$ for SOW8, $V_I = 5.5\text{V}$ , $T_J = 150^{\circ}\text{C}$ , $T_A = 25^{\circ}\text{C}$		/	264	mA
Maximum safety temperature		Ts	150	150	$^{\circ}\text{C}$
<b>UL1577</b>					
Insulation voltage per UL	$V_{\text{TEST}} = V_{\text{ISO}}$ , $t = 60\text{ s}$ (qualification), $V_{\text{TEST}} = 1.2 \times V_{\text{ISO}}$ , $t = 1\text{ s}$ (100% production test)	V <sub>ISO</sub>	3000	5000	V <sub>RMS</sub>

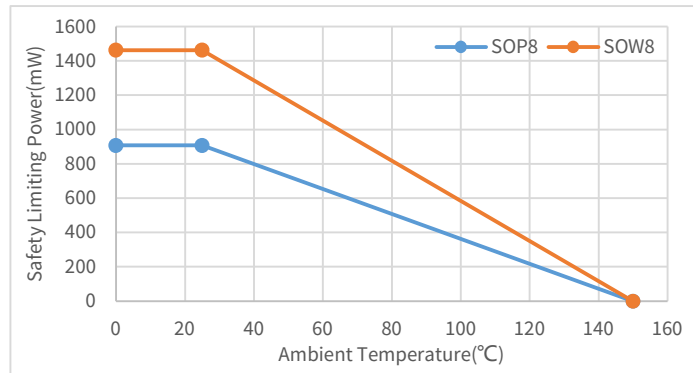


Figure 7.1 NSI1312x Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE 0884-17

### 7.3. Regulatory Information

The NSI1312x-DSWVR are approved or pending approval by the organizations listed in table.

UL		VDE	CQC
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1
Single Protection, 5000V <sub>rms</sub> Isolation voltage	Single Protection, 5000V <sub>rms</sub> Isolation voltage	Reinforce Insulation V <sub>IORM</sub> =2121Vpeak V <sub>IOTM</sub> =8000Vpeak V <sub>IOSM</sub> =10000Vpeak	Reinforced insulation
E500602	E500602	File (pending)	CQC20001264940

The NSI1312x-DSPR are approved or pending approval by the organizations listed in table.

UL		VDE	CQC
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1
Single Protection, 3000V <sub>rms</sub> Isolation voltage	Single Protection, 3000V <sub>rms</sub> Isolation voltage	Basic Insulation V <sub>IORM</sub> =990V <sub>peak</sub> V <sub>IOTM</sub> =4242V <sub>peak</sub> V <sub>IOSM</sub> =6000V <sub>peak</sub>	Basic insulation
E500602	E500602	File (pending)	CQC20001264940

## 8. Function Description

### 8.1. Overview

The NSI1312 is a cost-effective isolated amplifier with a high input impedance that accept wide range fully-differential input. The fully-differential input is suited to AC or bus voltage monitoring in high voltage applications where isolation is required. The analog input is continuously sampled by a second-order  $\Sigma$ - $\Delta$  modulator in the device. With the internal voltage reference and clock generator, the modulator converts the analog input signal to a digital bitstream, as shown in the Figure 8.1. The output of the modulator is transferred by the drivers (called TX in the Functional Block Diagram) across the isolation barrier that separates the isolated input side and output side voltage. The received bitstream and clock are synchronized and processed, as shown in the Functional Block Diagram, by a fourth-order analog filter on the output side and has a differential output. NSI1312 also has single-ended output version, as shown in the Figure 8.2, the received bitstream are processed and presented as a single-ended output with external voltage reference from REFIN pin.

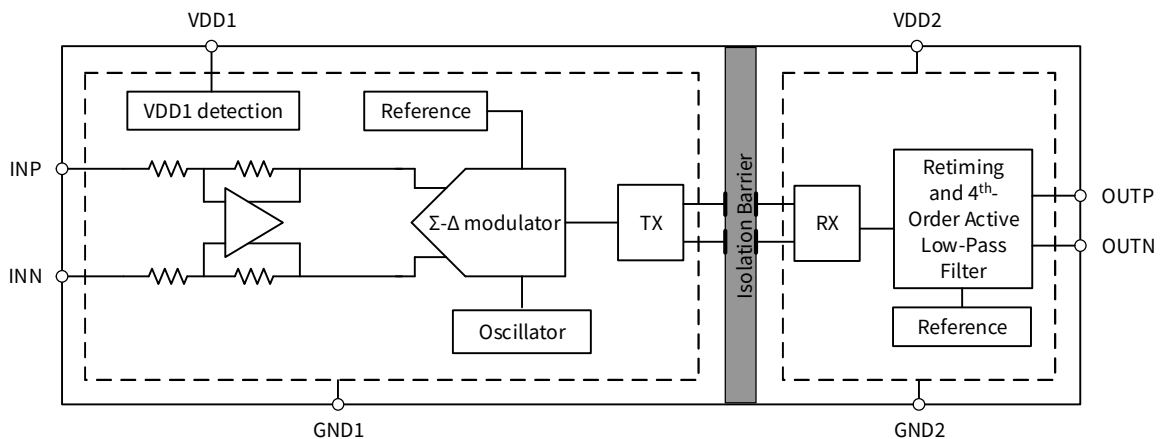


Figure 8.1 Function Block Diagram of Differential Output Version

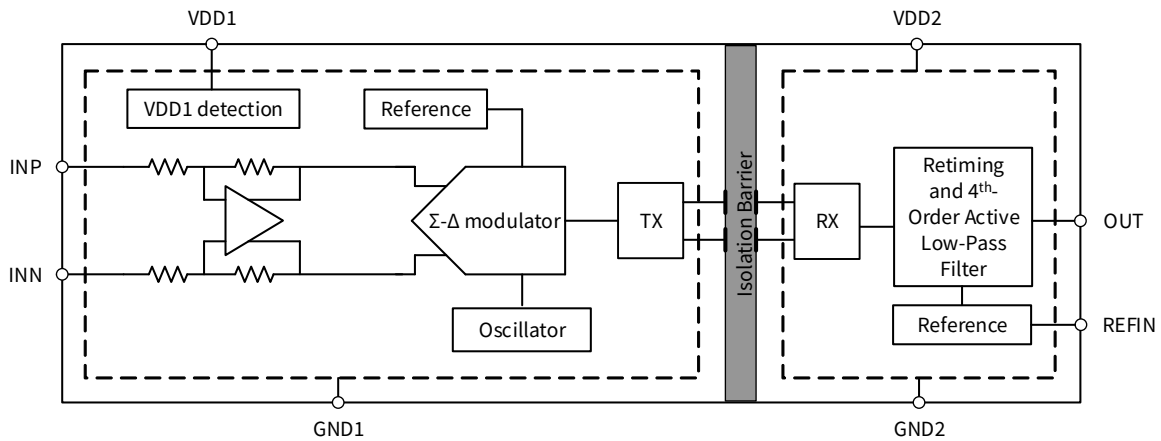


Figure 8.2 Function Block Diagram of Single-ended Output Version

### 8.2. Analog Input

There are two restrictions on the analog input signals (VINP and VINN).

- If the input voltage exceeds the range AGND – 6V to AVDD + 0.5V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on.
- The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

### 8.3. Analog Output

For linear input range, the analog output of NSI1312 has a fixed gain of 1. If a full-scale input signal is applied to the NSI1312 ( $V_{IN} \geq V_{Clipping}$ ), the differential analog output ( $V_{OUTP} - V_{OUTN}$  for NSI1312D and  $V_{OUT} - REF_{IN}$  for NSI1312S) will be clipped (typically, 1.44V for positive clipping and -1.44V for negative clipping). The negative clipping differential output waveform is shown in Figure 8.3.

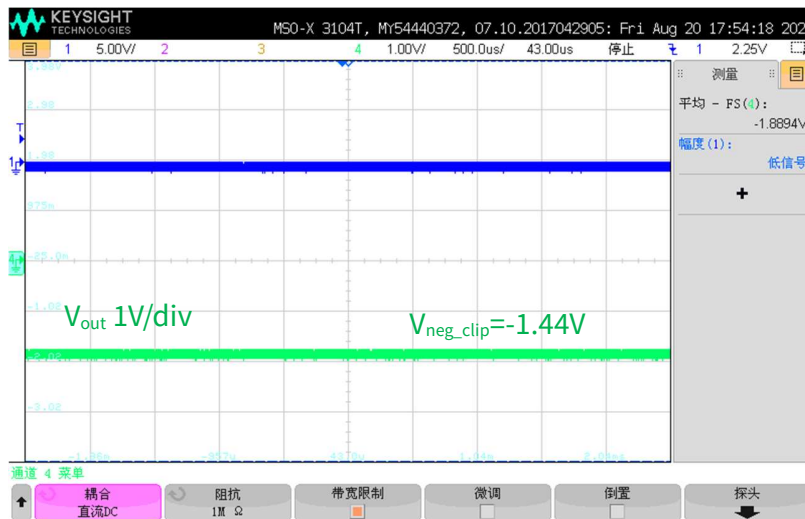


Figure 8.3 Typical negative clipping output

For differential output version (NSI1312D), the differential output pins have a common-mode voltage of 1.44V (typ). The differential output  $V_{out}$  of the NSI1312D is expressed as:

$$V_{out} = Gain * (V_{INP} - V_{INN})$$

For single-ended output version (NSI1312S), the REF<sub>IN</sub> pin with high input impedance needs external reference input. The output voltage  $V_{out}$  of the NSI1312S is expressed as:

$$V_{out} = Gain * (V_{INP} - V_{INN}) + REF_{IN}$$

In addition, NSI1312 integrates some diagnostic measures and offers a fail-safe output to simplify system-level design. The fail-safe output is a negative differential output voltage that does not occur under normal device operation, and it will only be activated when the undervoltage of VDD1 is detected ( $V_{DD1} < V_{DD1_{UV}}$ ). For NSI1312D, the typical failsafe output is  $-1.8V$  when VDD1 undervoltage, as is shown in Figure 8.4. For NSI1312S, the typical failsafe output is  $V_{failsafe} = 0V$  if  $V_{REF} < 1.8V$  and  $V_{failsafe} = V_{REF} - 1.8V$  if  $V_{REF} > 1.8V$  when VDD1 undervoltage, as is shown in Figure 8.5.

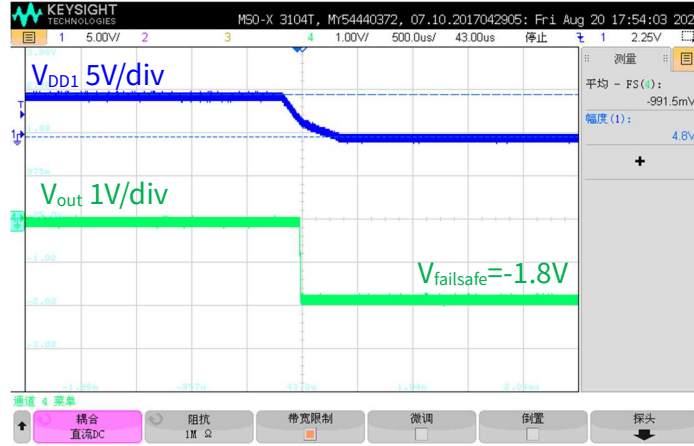
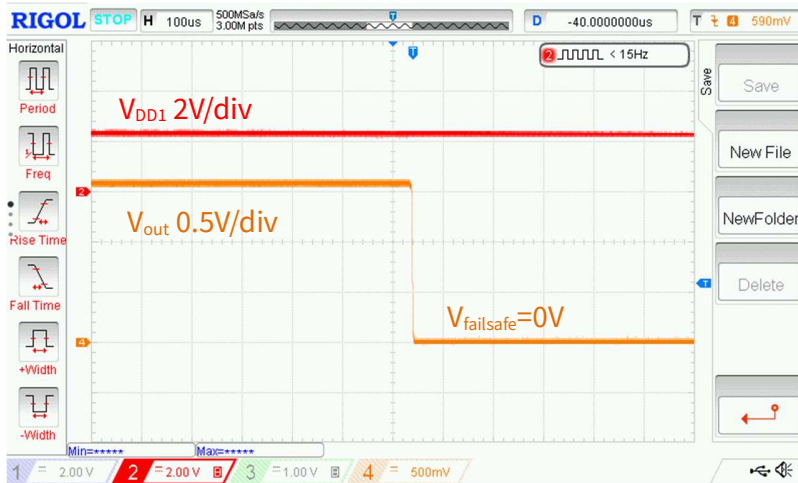
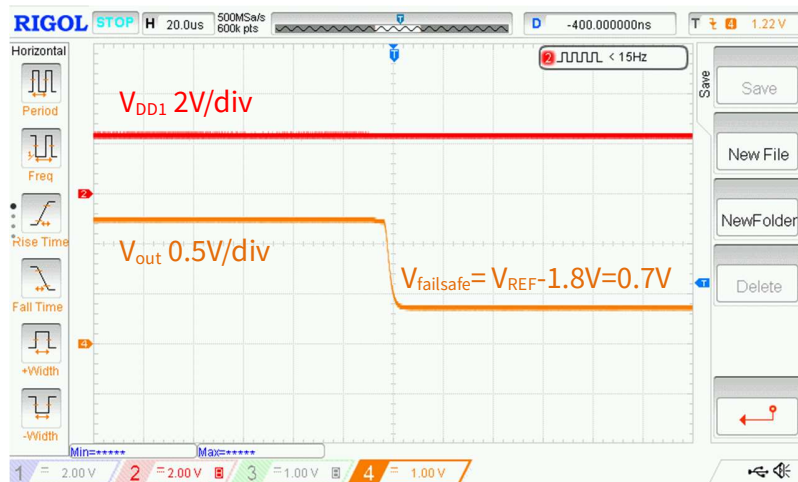


Figure 8.4 Typical Failsafe output when VDD1 undervoltage for NSI1312D



(a)  $V_{REF} = 1.6V$  ( $V_{REF} < 1.8V$ )



(b)  $V_{REF} = 2.5V$  ( $V_{REF} > 1.8V$ )

Figure 8.5 Typical failsafe output when VDD1 undervoltage for NSI1312S



## 9. Application Note

### 9.1. Typical Application Circuit

NSI1312 has an input impedance of up to 1MΩ, and has a wide bidirectional input voltage range as well. These features make NSI1312 ideally suitable for isolated AC and DC voltage sensing applications such as frequency inverters. The typical application circuit is shown in Figure 9.1.

For high voltage side design, the voltage of the frequency inverter is divided by a resistance network, and the divided voltage is applied to the input of NSI1312 through a RC filter to ensure best performance. The characteristics of this filter are dictated by the input topology and sampling frequency of the ADC, customer can adjust the filter design by demand. To reduce extra offset voltage caused by input bias current flowing through  $R_{sense}$ , suggest to add  $R_{FLTP}$  as below. To reduce extra gain error caused by input resistance of NSI1312, suggest customer to choose smaller resistance, such as  $R_{sense} \leq 10k\Omega$ .

About controller side design, for differential output version (NSI1312D), the differential output of the isolated amplifier is converted to a single-ended analog output with an operational-amplifier-based circuit. Suggest to add >1kΩ resistor on the OUTP and OUTN pin to prevent output over-current protection.

For single-ended output version (NSI1312S), REFIN needs external reference input, such as accurate reference IC, LDO and resistor divider network. The single-ended output swing range is  $GND2+0.3V-VDD2-0.3V$ . To avoid OUT clamp, REFIN is recommended to be taken as  $VDD2/2$  if need to support  $\pm 1.2V$  analog input range. If the reference is noisy, customer need to add RC filter and adjust the value by demand. The output can be connected to an analog-to-digital converter without signal conditioning. An analog-to-digital converter usually receives the analog output and converts to digital signal for controller processing.

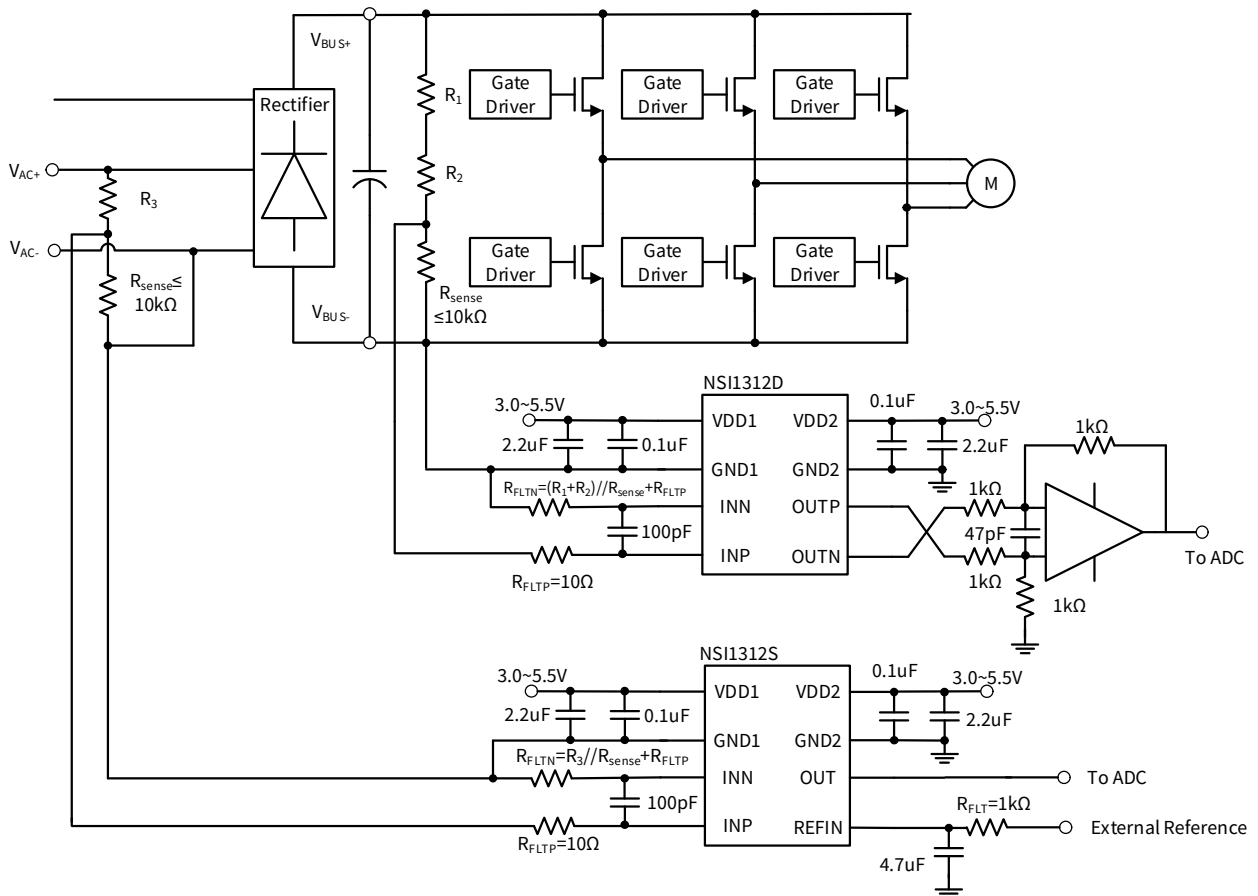


Figure 9.1 Typical application circuit in voltage sensing

### 9.2. Sense Resistor Selection

There are two other factors should be considered when selecting the sense resistor:

- The voltage-drop on  $R_{sense}$  divided by nominal  $V_{BUS}$  or  $V_{AC}$  must not exceed the recommended linear input voltage range:  $V_{IN} \leq FSR$ .
- The voltage-drop on  $R_{sense}$  divided by  $V_{BUS}$  or  $V_{AC}$  in maximum allowed overvoltage condition must not exceed the input voltage that causes a clipping output:  $V_{IN} \leq V_{clipping}$ .

**9.3. PCB Layout**

There are some key guidelines or considerations for optimizing performance in PCB layout:

- NSI1312 requires a 0.1 $\mu$ F bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the VDD pin. If better filtering is required, an additional 1~10 $\mu$ F capacitor may be used.
- Kelvin rules is recommended for the connection between shunt resistor to NSI1312. Because of the Kelvin connection, any voltage drops across the trace and leads should have no impact on the measured voltage.
- Place the shunt resistor close to the INP and INN inputs and keep the layout of both connections symmetrical and run very close to each other to the input of the NSI1312. This minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal.

**10. Package Information**

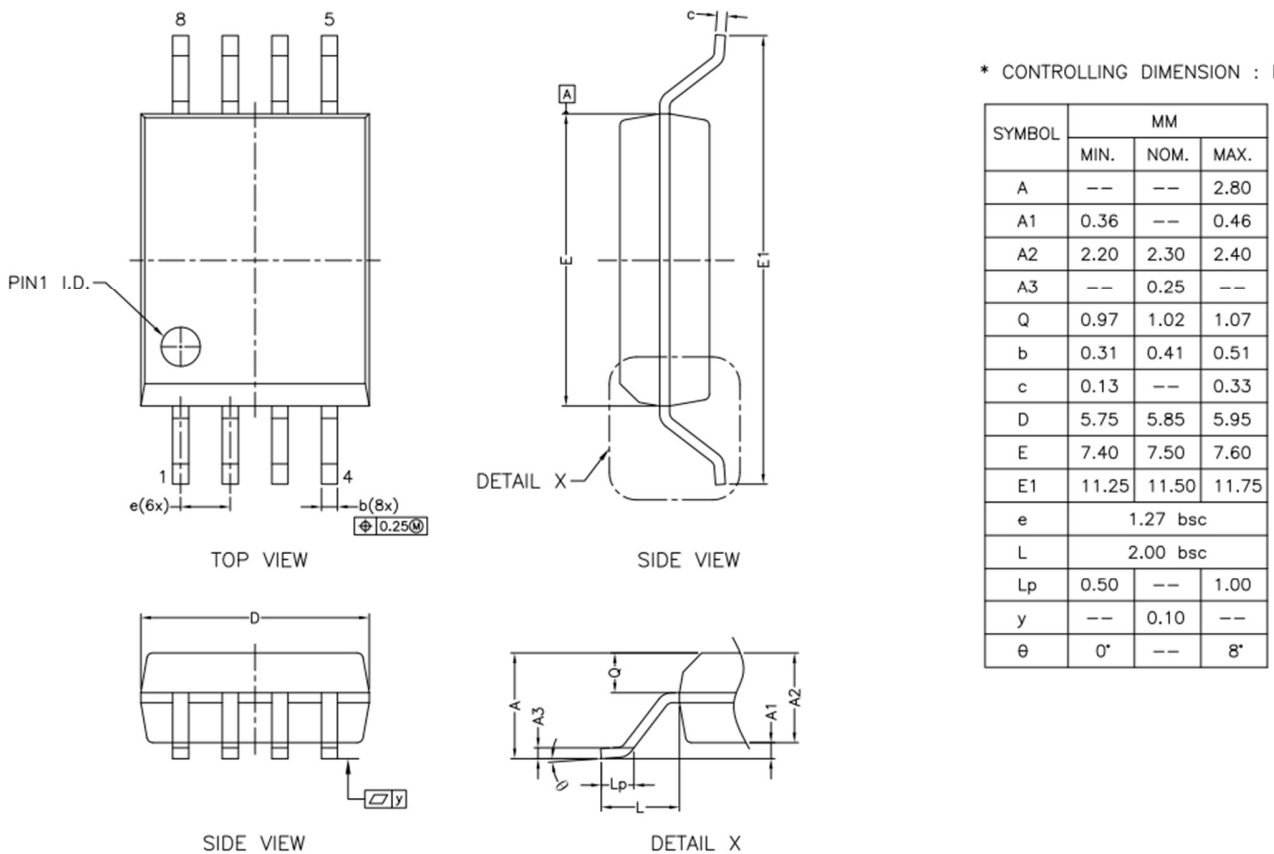
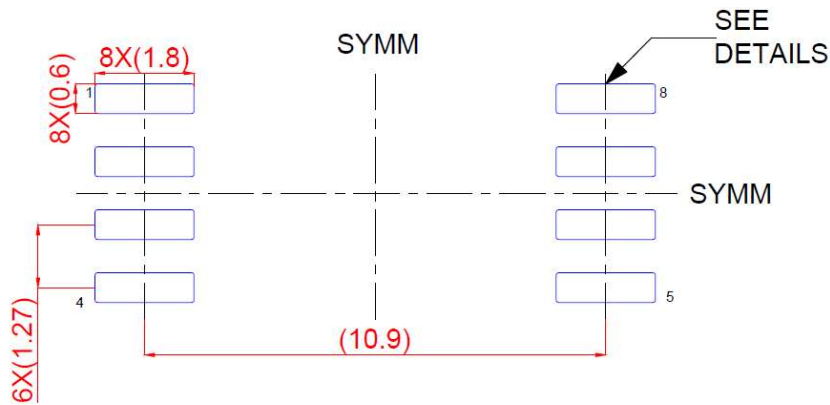


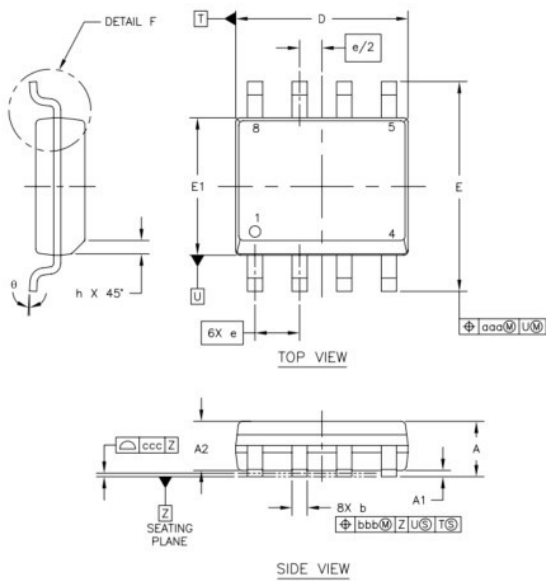
Figure 10.1 SOW8 Package Shape and Dimension in millimeters



LAND PATTERN EXAMPLE(mm)  
9.1 mm NOMINAL  
CLEARANCE/CREEPAGE

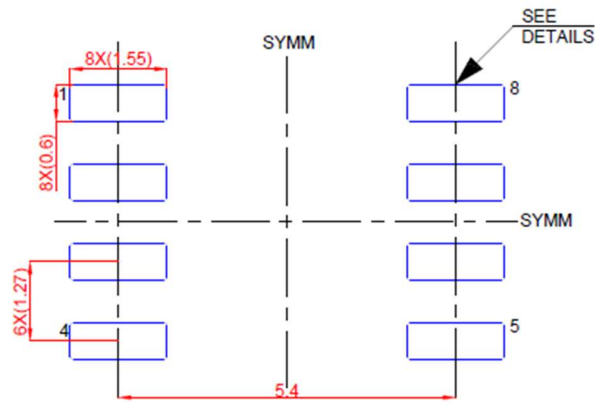


Figure 10.2 SOW8 Package Board Layout Example

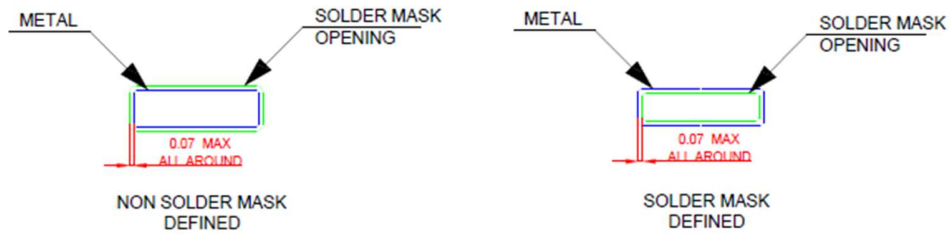


DESCRIPTION	SYMBOL	INCH			MILLIMETER		
		MIN	NOM	MAX	MIN	NOM	MAX
TOTAL THICKNESS	A	.053		.069	1.35		1.75
STAND OFF	A1	.004		.010	0.10		0.25
MOLD THICKNESS	A2	.049		---	1.25		---
LEAD WIDTH	b	.014		.019	0.35		0.49
L/F THICKNESS	c	.007		.010	0.19		0.25
BODY SIZE	D	.189		.197	4.80		5.00
	E1	.150		.157	3.80		4.00
	E	.228		.244	5.80		6.20
LEAD PITCH	e	.050 BSC			1.27 BSC		
	L	.016		.049	0.40		1.25
	h	.010		.020	0.25		0.50
	θ	0°		7°	0°		7°
	θ1	5°		15°	5°		15°
	θ2	2°		7°	2°		7°
LEAD EDGE OFFSET	aaa	.010			0.25		
LEAD OFFSET	bbb	.010			0.25		
COPLANARITY	ccc	.004			0.10		

Figure 10.3 SOP8 package shape and dimension in millimeters



LAND PATTERN EXAMPLE(mm)



SOLDER MASK DETAILS

Figure 10.4 SOP8 Package Board Layout Example

## 11. Ordering Information

<b>Part No.</b>	<b>Isolation Rating(kV)</b>	<b>Linear Input Range(V)</b>	<b>Moisture Sensitivity Level</b>	<b>Temperature</b>	<b>Automotive</b>	<b>Package Type</b>	<b>Package Drawing</b>	<b>SPQ</b>
NSI1312D-DSPR	3	-1.2 ~ 1.2	Level-3	-40 to 125°C	NO	SOP8 (150mil)	SOP8	2500
NSI1312S-DSPR	3	-1.2 ~ 1.2	Level-3	-40 to 125°C	NO	SOP8 (150mil)	SOP8	2500
NSI1312D -DSWVR	5	-1.2 ~ 1.2	Level-3	-40 to 125°C	NO	SOP8 (300mil)	SOW8	1000
NSI1312S -DSWVR	5	-1.2 ~ 1.2	Level-3	-40 to 125°C	NO	SOP8 (300mil)	SOW8	1000

## 12. Documentation Support

<b>Part Number</b>	<b>Product Folder</b>	<b>Datasheet</b>	<b>Technical Documents</b>	<b>Isolator selection guide</b>
NSI1312	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 13. Tape and Reel Information

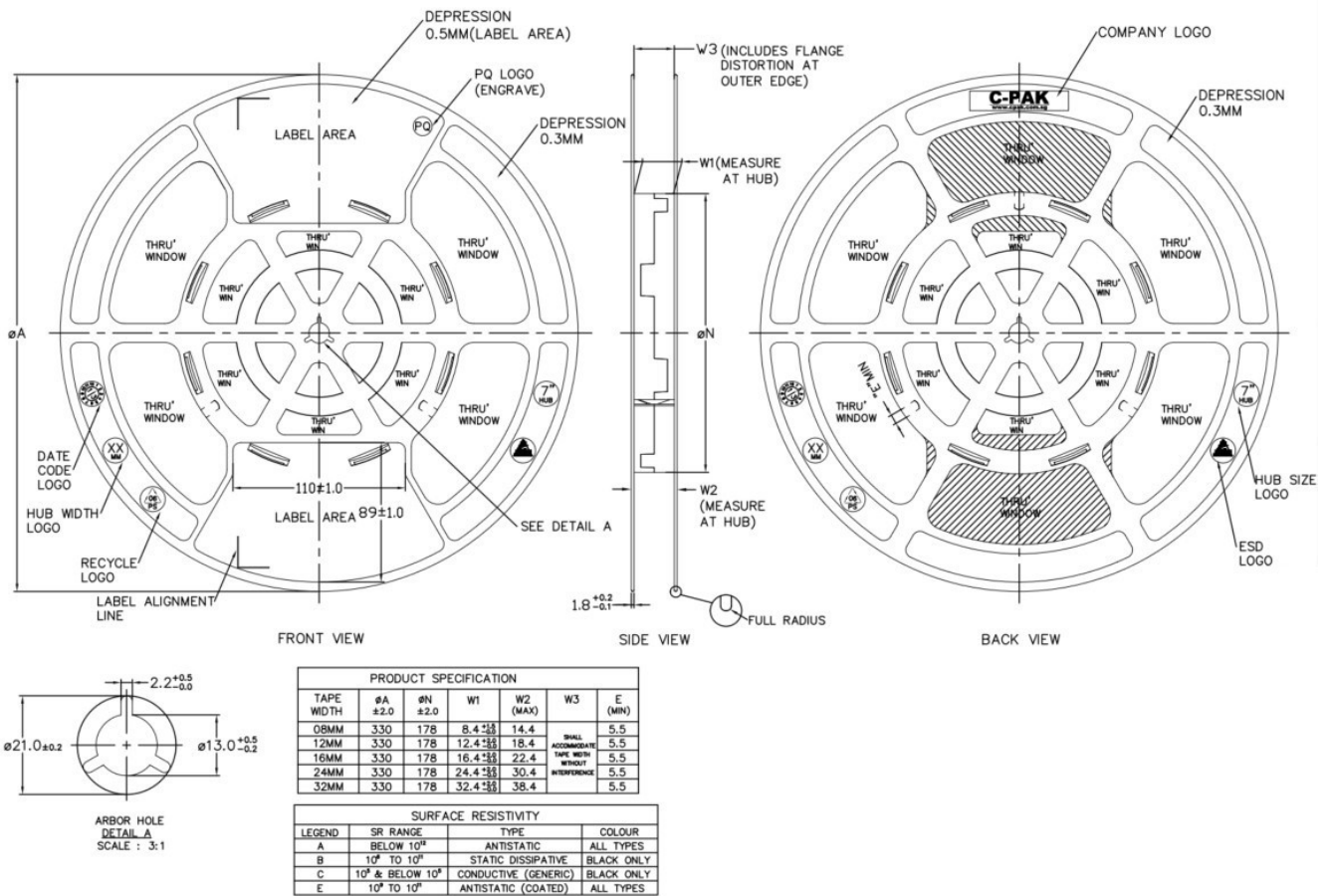


Figure 13.1 Tape Information

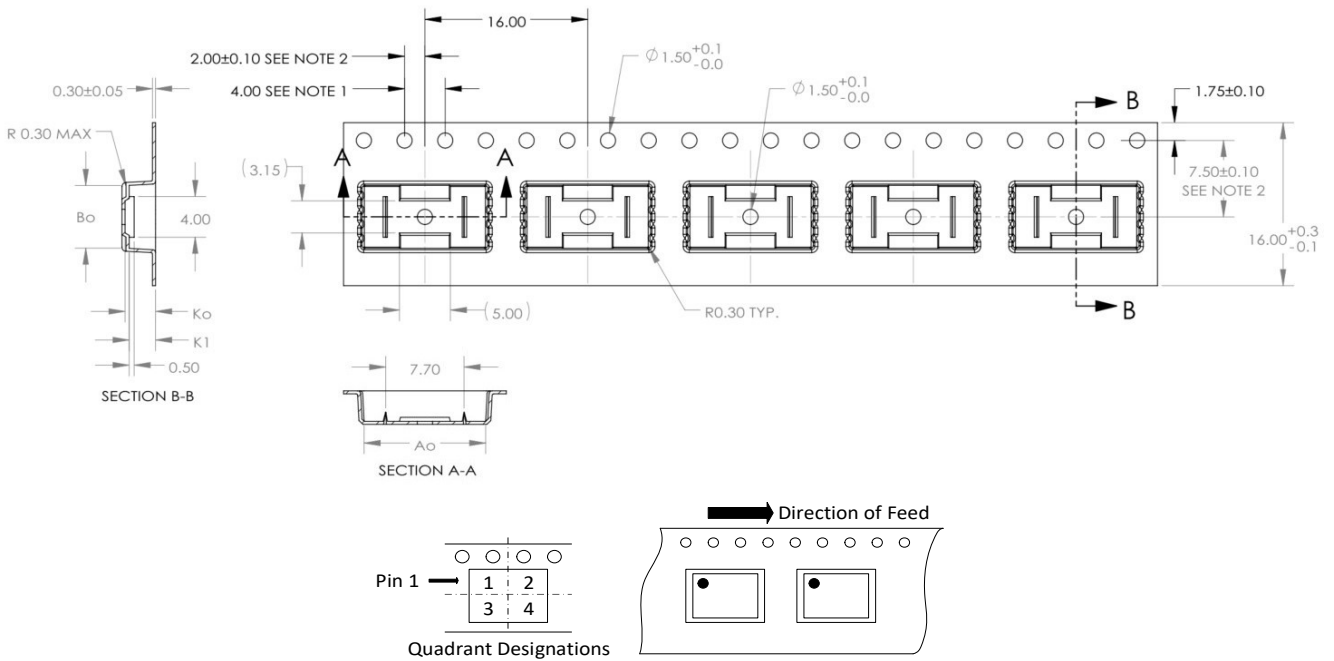


Figure 13.2 Reel Information of SOP8(300mil)

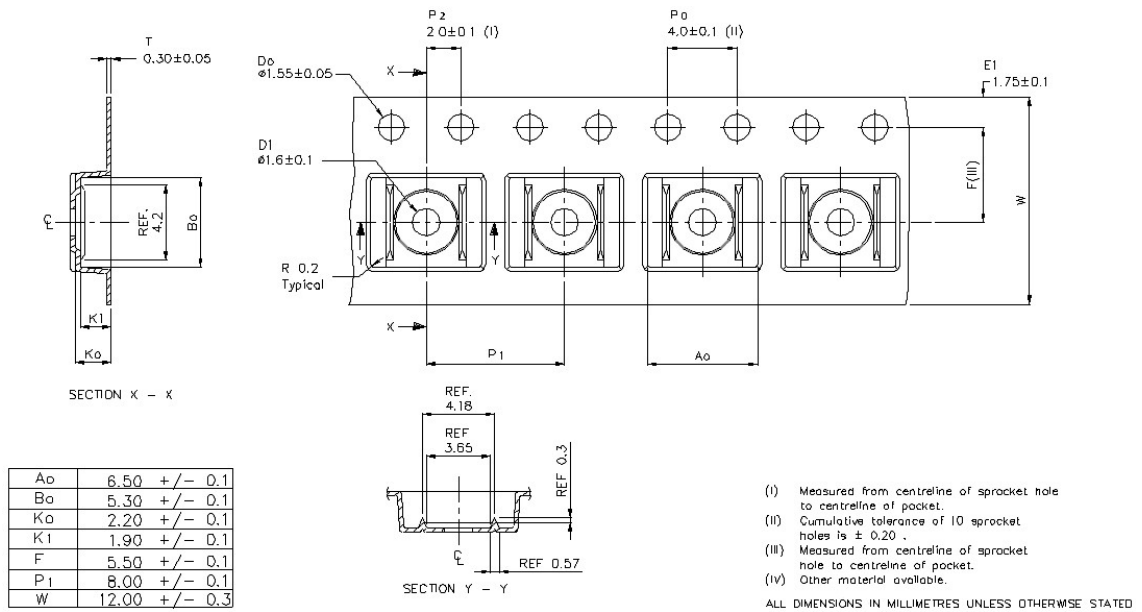


Figure 13.3 Reel Information of SOP8(150mil)

## 14. Revision History

Revision	Description	Date
1.0	Initial Release	2022/3/23
1.1	Update REFIN specification in 5.2 and UL certificate number in 6.3 and input filter resistance in Fig 8.1	2022/6/27
1.2	Update $V_{CM}$ range in part 3, $V_{FAILSAFE}$ and $PSRR_{AC}$ specifications in 5.1, the comments of $V_{OS}$ , $I_{IB}$ , $E_G$ and Nonlinearity in 5.1, Figure 5.11~5.14 in 5.3, the standard on which $V_{IOSM}$ test method is based in 6.2, CQC certificate number in 6.3, description for analog output of NSI1312S in 7.3 and input filter resistance in Fig 8.1. Update typeface to Source Sans Pro.	2022/12/24
1.3	<ul style="list-style-type: none"> <li>● Updated the description of isolation level in the header of first page from 'Reinforced' to "Reinforced/Basic";</li> <li>● Updated specifications in Key features;</li> <li>● Updated Offset Error from <math>\pm 5mV</math> to <math>\pm 2.5mV</math> in Section. 6.1;</li> <li>● Updated Offset Drift from <math>\pm 25\mu V/^{\circ}C</math> (Typ) to <math>\pm 20\mu V/^{\circ}C</math> (Max) in Section. 6.1;</li> <li>● Updated Gain Error from <math>\pm 0.4\%</math> to <math>\pm 0.3\%</math> in Section. 6.1;</li> <li>● Updated Gain Error Drift from <math>\pm 50ppm/^{\circ}C</math> (Typ) to <math>\pm 40ppm/^{\circ}C</math> (Max) in Section. 6.1;</li> <li>● Updated THD from -70dB to -75dB in Section. 6.1;</li> <li>● Added a separate section of ESD ratings and changed its description;</li> <li>● Updated ESD the level of HBM from <math>\pm 2.0kV</math> to <math>\pm 4.0kV</math>;</li> <li>● Updated the lower limit of VDD1 power supply from 4.5V to 3.0V in Pin Configuration and Functions;</li> <li>● Updated the description of Safety Regulation Approvals;</li> <li>● Updated the description of Safety certification in Section.7(Section.6 in previous edition).</li> </ul>	2023/7/20



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